RECEIVED
CENTRAL FAX CENTER

Patent

FEB 14 2006

Attorney Docket No.: Intel 2207/1211902
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT   :   James BREISCH et al.

SERIAL NO.   :   10/662,391

FILED   :   September 16, 2003

FOR   :   DUAL REFERENCED MICROSTRIP

GROUP ART UNIT   :   2815

EXAMINER   :   Jesse A. FENTY

CUSTOMER NO.   :   25693

M/S: APPEAL BRIEFS – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
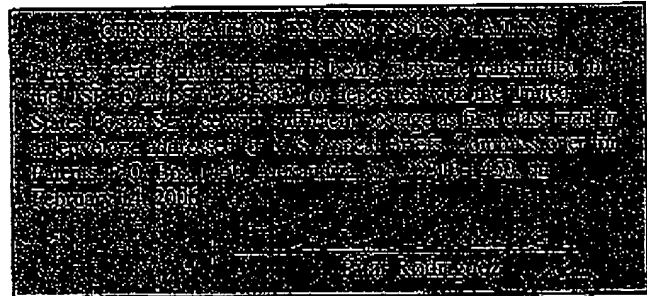
APPEAL BRIEF

Dear Sir:

This brief is in furtherance of the Notice of Appeal, filed in this case on November 14,

2005.

1.   REAL PARTY IN INTEREST

The real party in interest in this matter is Intel Corporation. (Recorded April 5, 2002,

Reel/Frame 012776/0940).

Serial No. 10/662,391
Appeal Brief Under 37 CFR 41.37 Filed February 14, 2006
Advisory Action dated November 1, 2005

2.   RELATED APPEALS AND INTERFERENCE

There are no related appeals.

3.   STATUS OF THE CLAIMS

Claims 1-14 are pending in this application. Claims 1-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Koontz et al. (U.S. Patent No. 6,181,004 B1) (hereinafter "Koontz").

4.   STATUS OF AMENDMENTS

Applicants did not make any amendments to the claim subsequent to final rejection. The claims listed on page 1 of the Appendix attached to this Appeal Brief reflect the present status of the claims (including amendments entered after final rejection).

5.   SUMMARY OF THE CLAIMED SUBJECT MATTER

The embodiment of claim 1 generally describes a semiconductor package, comprising: a dual referenced transmission line having a predefined characteristic impedance and characteristic impedance tolerance value (e.g., *see* page 7, paragraph 27 – Figure 3, 300); a first conductive plane (e.g., *see* page 7, paragraph 26 – Figure 3, 302); a first dielectric layer provided between the dual referenced transmission line and the first conductive plane (e.g., *see* page 7, paragraph 26 – Figure 3, 304); a second conductive plane; a second dielectric layer provided between the first conductive plane and the second conductive plane (e.g., *see* page 7, paragraph 26 – Figure 3, 308), wherein an inter-plane impedance is an impedance of the first conductive plane with reference to the second conductive plane (e.g., *see* page 6, paragraph 25); and wherein at least

2

one physical parameter associated with the inter-plane impedance is selected such that the

characteristic impedance value of the dual referenced transmission line does not exceed the

characteristic impedance tolerance value with respect to the first and second conductive planes

(e.g., *see* page 6, paragraph 43).

A dual referenced transmission line having predefined characteristic impedance and

characteristic impedance tolerance values (e.g., *see* page 7, paragraph 27 – Figure 3, 300), the

dual referenced transmission line for transmission of a signal in a package including

semiconductor circuits, wherein the dual referenced transmission line is comprised of: a signal

routing trace (e.g., *see* page 7, paragraph 30 – Figs. 4A and 4B, 318) positioned over a first

reference plane (e.g., *see* page 8, paragraph 30 - Figs. 4A and 4B, 322), which is in turn

positioned over a second reference plane (e.g., *see* page 8, paragraph 30 - Figs. 4A and 4B, 314),

wherein an inter-plane impedance is an impedance of the first reference plane with reference to

the second reference plane (e.g., *see* page 8, paragraph 30); and wherein at least one physical

parameter associated with the inter-plane impedance is selected such that the characteristic

impedance value of the dual referenced transmission line does not exceed the characteristic

impedance tolerance value with respect to the first and second reference planes (e.g., *see* page 6,

paragraph 43).

FIG. 1 illustrates a typical die/package/printed circuit board interface. The die 100 may

interface to the package 102 on a first side 104 of the package 102. The interface may be

achieved, for example, by a plurality of solder bumps 106 in a die/package interface area. The

die/package interface area is very congested; the solder bumps 106 may have a pitch of even

smaller than 200 μm. Signal paths (e.g., system bus traces or IO traces) typically fan out from

the congested die/package interface area to the balls of a BGA 108 (or lands in a PGA, not

shown). The BGA 108 is typically on a second side 110 of the package 102, the second side 110 being opposite to the first side 104.

FIG. 2 illustrates a "dual referenced microstrip" configuration 200 according to an embodiment of the present invention. A microstrip configuration 202 may be characterized by a signal path routing layer 204, supported by a first dielectric 206 adjacent to a primary reference layer 208. The signal path routing layer 204 is easily accessible. In a dual referenced microstrip configuration 200, a secondary reference layer 210 is positioned adjacent to the primary reference layer 208 and separated therefrom by a second dielectric layer 212. A problem with this configuration, however, has been that the characteristic impedance of the signal path routing layer 204, referenced to the primary reference layer 208 was generally believed to be different from the characteristic impedance of the signal path routing layer 204 referenced to the secondary reference layer 210; this difference was unpredictable and could vary according to manufacturing techniques, among other things.

FIG. 3 illustrates an example of a six-layer package stackup 300 including a dual referenced microstrip transmission line in the signal path routing layer 318 (similar to 204 FIG. 2). The package stackup 300 includes: a bottom conductive plane 302, which may be used for example, for LGA/Routing; a first dielectric layer 304; a ground layer 306, which may be a VSS plane; a second dielectric layer 308, a power plane layer 310, which may be a VCC plane; a dielectric core 312; a secondary reference layer 314, which may be a power plane (e.g., VCC) layer; a third dielectric layer 316; a primary reference layer 322, which may be a ground plane (e.g., VSS) layer; a fourth dielectric layer 320, and a signal routing layer 318.

FIG. 4A illustrates a first return path 402 and a second return path 404 through which return current may flow if the signal path 318 is referenced to the primary reference layer 322.

4

FIG. 4B illustrates a third return path 406 and a fourth return path 408 through which return current may flow if the signal path 318 is referenced to the secondary reference layer 314. In FIGS. 4A and 4B, the dielectric layers 316 and 320 have been omitted for clarity.

FIG. 5 is a flowchart presenting a method of designing a dual referenced microstrip transmission line. The method may start at step 500. At step 502, the impedance of the dual referenced transmission line 318 referenced to the primary reference plane 322 may be calculated. The characteristic impedance may be calculated according to the equation set forth above, specifically, $Z_{01} = (Z_{SECONDARY} + Z_{INTER-PLANE}) \| Z_{PRIMARY}$, where Z_{01} represents the characteristic impedance of the transmission line referenced to the primary reference plane. At step 504, the characteristic impedance of the dual referenced transmission line 318 referenced to the secondary reference plane 314 is calculated. The characteristic impedance may be calculated according to the equation set forth above, specifically, $Z_{02} = (Z_{PRIMARY} + Z_{INTER-PLANE}) \| Z_{SECONDARY}$, where Z_{02} represents the characteristic impedance of the transmission line referenced to the secondary reference plane. Of course, other equations may be used to arrive at the characteristic impedances of Z_{01} and/or Z_{02}. At step 506, the absolute value of the difference between Z_{01} and Z_{02} may be calculated. At step 508, the calculated absolute value of the difference is compared to a predetermined threshold value; if the absolute value of the difference is greater than the predetermined threshold value, then, at step 510, at least one physical parameter associated with the impedance between the two reference planes may be adjusted. In accordance with one exemplary embodiment of the invention, the predetermined threshold value may be less than 2 Ohms for frequencies less than 1 GHz. Physical parameters that may be adjusted include, but are not limited to the thickness of the dielectric layer separating the two reference planes; the relative

5

dielectric constant of the dielectric separating the two reference planes; the surface area of the

adjacent reference planes; the thickness of the conductive reference plane materials; the type of

conductive reference plane materials; placement of discrete capacitors shunting the two reference

planes; and the number of connections (e.g., number of balls in the BGA) which the package

makes to the die and printed circuit board. After step 510, the method may return to step 502. If

the absolute value of the difference between Z_{01} and Z_{02} is less than or equal to the

predetermined threshold value, then the method may end at step 512.

FIG. 6 is a representation of a stackup of layers as used in a computer simulated circuit

in accordance with an embodiment of the invention;

FIG. 7 is a graphic representation of the results of a first simulation using the stackup of

FIG. 6, in accordance with an embodiment of the invention; and

FIG. 8 is a graphic representation of the results of a second simulation using the stackup

of FIG. 6, in accordance with an embodiment of the invention.

6.   GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A.   Claims 1-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over

Koontz et al. (U.S. Patent No. 6,181,004 B1) (hereinafter "Koontz").

7.   ARGUMENT

A.   Claims 1-14 are not rendered obvious under 35 U.S.C. § 103(a) by Koontz

Applicants respectfully submit the cited reference Koontz does not teach, suggest or

disclose "[a] semiconductor package, comprising: a dual referenced transmission line having a

6

Serial No. 10/662,391
Appeal Brief Under 37 CFR 41.37 Filed February 14, 2006
Advisory Action dated November 1, 2005

predefined characteristic impedance and characteristic impedance tolerance value ... *and wherein at least one physical parameter associated with the inter-plane impedance is selected such that the characteristic impedance value of the dual referenced transmission line does not exceed the characteristic impedance tolerance value with respect to the first and second conductive planes"* (e.g., as described in claim 1).

First, Applicants concur with the Examiner's assertion that Koontz does not expressly disclose at least the selection of a parameter associated with inter-plane impedance such that the impedance value of the dual referenced transmission line does not exceed a characteristic impedance tolerance value. *See* Office Action dated 6/14/2005, paragraph 2.

As argued below, Applicants submit that the structure described in Koontz is inadequate to support a proper § 103(a) rejection for at least the following reasons:

a)   the structure disclosed in Koontz is insufficient to support a proper § 103(a) rejection;

b)   the cited reference Koontz does not teach, suggest or disclose "dual referenced transmission lines" as described in embodiments of the present application; and

c)   the two structures (the Koontz structure vs. embodiments of the present application) are so different that one of ordinary skill in the art would not have been motivated to so drastically change, if possible, the Koontz structure so as to arrive at the claimed invention.

First, Applicants note Koontz does not relate to, and does not consider, dual referenced transmission lines. The physical structure (i.e., the stackup) of a dual referenced transmission line is fundamentally different from the physical structure of the "multilayer module 50" of Koontz.

The Examiner, however, considers Koontz structure to be relevant. Applicants disagree

and present a side-by-side comparison of the two structures:
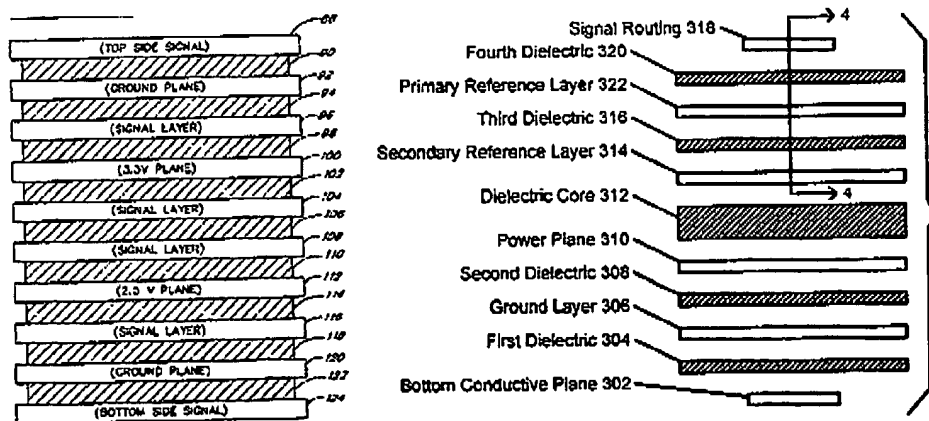
As is seen from the side-by-side illustrations above, the structure of Koontz is missing, at least, a

secondary reference layer (i.e., a reference plane) beneath Ground Plane 92. The layer beneath

Koontz's Ground Plane 92 is a signal plane, which is identified as Signal Layer 96. Signal Layer

96 cannot be considered as a *reference* plane within the ordinary meaning of the term.

Therefore, Applicants submit since the structure disclosed in Koontz does not reflect the *"dual*

referenced transmission lines" as specifically recited in embodiments of the present invention,

Koontz is inadequate to support a proper §103(a) rejection.

Moreover, the Office Action asserts that Koontz discusses the controlling and matching

of the impedance of the ground and signal layers (column 7, lines 8-16) and asserts it would have

been obvious to one of ordinary skill in the art at the time to vary the relative impedances of

various layers with regard to one another for the purpose of providing a clearer signal and a more

predictable result. Column 7, lines 8-16 state:

> The impedance of the signal lines on a conductive layer may be
> controlled by the thickness and type of dielectric material used in the
> insulation layer and by the thickness and width of the metallization of the
> conductive layer using known techniques. By positioning signal layers on

opposite sides of the ground layers, and by selecting the type and thickness of the dielectric between the ground layer and the two signal layers, the impedance of the signal layers may be controlled and matched.

Applicants respectfully assert that Koontz teaches "positioning signal layers on opposite sides of the ground layers [adjacent to the signal layers]." The signal layers referred to are the Top Side Signal 88 and the Signal Layer 96. Koontz emphasizes that placing signal layers on opposite sides of a ground layer will prevent cross-talk between signal lines on each of the signal layers. However, *dual referenced transmission lines* do not position signal layers on opposite sides of ground layers as described and illustrated in Koontz.
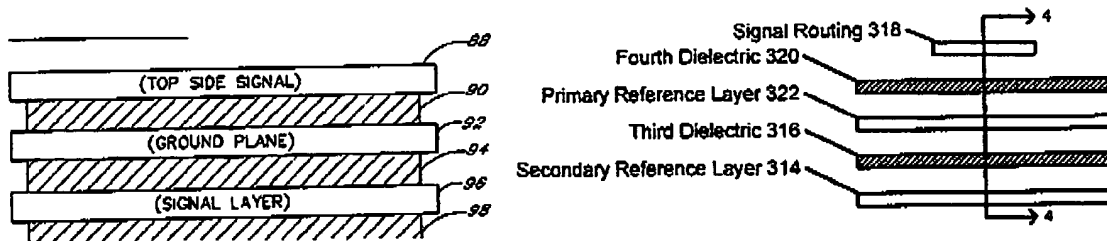
Koontz teaches that the impedance of a first signal line on Top Side Signal 88 (with reference to the Ground Plane 92) is distinct from, and independent of, the impedance of a second signal line on Signal Layer 96 (with reference to the Ground Plane 92). Note that Koontz relates to a structure where there are two signal lines; a first and a second; one on top and a second below a single shared ground plane.

Dual reference transmission lines (as described in embodiments of the present application), on the other hand, relates to a structure with one signal line. The impedance of the one signal line with reference to the Primary Reference Layer 322 may be different from the impedance of the same signal line with reference to the Secondary Reference Layer 314. The claimed invention is not described by Koontz, which offhandedly comments on the impedance of

-9-

first and second signal lines that share a single reference plane (i.e., Ground Plane 92)

sandwiched between them.

Therefore, in addition to not disclosing the relevant limitations discussed above,

Applicants submit that the two structures (Koontz vs. the claimed invention) are so different that

one of ordinary skill in the art simply could not find a motivation in Koontz to so drastically

change its structure as to arrive at the claimed invention.

In order for a 103(a) rejection to succeed, each and every limitation of independent claim

1 must be in the cited references. For the reasons cited above, Koontz fails to disclose each and

every element of independent claim1. Since each and every limitation is not found in the cited

references, the 103(a), claim 1 is allowable and the 103(a) rejection should be withdrawn.

Independent claim 4 contains similar allowable limitations. Claims 2, 3 and 5-14 are allowable

for depending from allowable base claims.

Appellants therefore respectfully request that the Board of Patent Appeals and

Interferences reverse the Examiner's decision rejecting claims 1-19 and direct the Examiner to

pass the case to issue.

Serial No. 10/662,391
Appeal Brief Under 37 CFR 41.37 Filed February 14, 2006
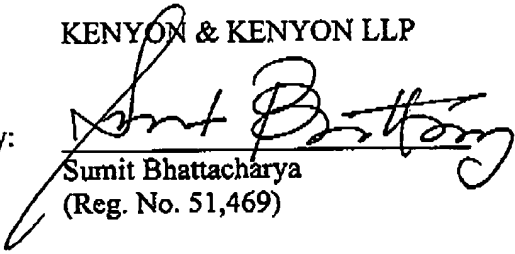Advisory Action dated November 1, 2005

   The Examiner is hereby authorized to charge the appeal brief fee of **$500.00** and any

additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon

Deposit Account No. **11-0600**.

              Respectfully submitted,

              KENYON & KENYON LLP

Date: <u>February 14, 2006</u>   By: _____
               Sumit Bhattacharya
               (Reg. No. 51,469)

KENYON & KENYON LLP
333 West San Carlos St., Suite 600
San Jose, CA 95110
Telephone: (408) 975-7500
Facsimile: (408) 975-7501

82276.1

<div align="center">-11-</div>

Serial No. 10/662,391
Appeal Brief Under 37 CFR 41.37 Filed February 14, 2006
Advisory Action dated November 1, 2005

APPENDIX

(Brief of Appellants James BREISCH et al.
U.S. Patent Application Serial No. 10/662,391)

8. CLAIMS ON APPEAL

1.   (Previously presented) A semiconductor package, comprising:

a dual referenced transmission line having a predefined characteristic impedance and characteristic impedance tolerance value;

a first conductive plane;

a first dielectric layer provided between the dual referenced transmission line and the first conductive plane;

a second conductive plane;

a second dielectric layer provided between the first conductive plane and the second conductive plane, wherein an inter-plane impedance is an impedance of the first conductive plane with reference to the second conductive plane; and

wherein at least one physical parameter associated with the inter-plane impedance is selected such that the characteristic impedance value of the dual referenced transmission line does not exceed the characteristic impedance tolerance value with respect to the first and second conductive planes.

2.   (Previously presented) The semiconductor package of claim 1, wherein an absolute value of a difference between a characteristic impedance of the dual referenced transmission line referenced to the first conductive plane and a characteristic impedance of the dual referenced transmission line referenced to the second conductive plane is less than the predetermined characteristic impedance tolerance value.

3.   (Previously presented) The semiconductor package of claim 1, wherein the characteristic impedance of the dual referenced transmission line is calculated as a function of at least one physical parameter associated with the inter-plane impedance.

-1-

4.   (Previously presented) A dual referenced transmission line having predefined characteristic impedance and characteristic impedance tolerance values, the dual referenced transmission line for transmission of a signal in a package including semiconductor circuits, wherein the dual referenced transmission line is comprised of: a signal routing trace positioned over a first reference plane, which is in turn positioned over a second reference plane, wherein an inter-plane impedance is an impedance of the first reference plane with reference to the second reference plane; and

wherein at least one physical parameter associated with the inter-plane impedance is selected such that the characteristic impedance value of the dual referenced transmission line does not exceed the characteristic impedance tolerance value with respect to the first and second reference planes.

5.   (Previously presented) The dual referenced transmission line of claim 4, wherein an absolute value of a difference between a characteristic impedance of the signal routing trace referenced to the first reference plane and a characteristic impedance of the signal routing trace referenced to the second reference plane is less than the predetermined characteristic impedance tolerance value.

6.   (Previously presented) The dual referenced transmission line of claim 4, wherein the characteristic impedance of the signal routing trace is calculated as a function of at least one physical parameter associated with the inter-plane impedance.

7.   (Previously presented) The semiconductor package of claim 2, wherein the predetermined characteristic impedance tolerance value is two Ohms.

8.   (Previously presented) The semiconductor package of claim 1, wherein the dual referenced transmission line characteristic impedance tolerance value is proportional to the inter-plane impedance.

9.   (Previously presented) The semiconductor package of claim 1, wherein the dual referenced transmission line characteristic impedance tolerance value is directly proportional to the inter-plane impedance.

10.   (Previously presented) The semiconductor package of claim 1, wherein the physical parameter associated with the inter-plane impedance is at least one of: thickness of the second dielectric layer; the relative dielectric constant of the second dielectric layer; the surface area of the first and second conductive planes; the thickness of the conductive material of the first or second conductive planes; the type of conductive material of the first or second conductive planes; placement of discrete capacitors shunting the first and second conductive planes; and the number of connections which the semiconductor package makes to a die and a printed circuit board.

11.   (Previously presented) The dual referenced transmission line of claim 5, wherein the predetermined characteristic impedance tolerance value is two Ohms.

12.   (Previously presented) The dual referenced transmission line of claim 4, wherein the characteristic impedance tolerance value is proportional to the inter-plane impedance.

13.   (Previously presented) The dual referenced transmission line of claim 4, wherein the characteristic impedance tolerance value is directly proportional to the inter-plane impedance.

14.   (Previously presented) The dual referenced transmission line of claim 4, wherein the physical parameter associated with the inter-plane impedance is at least one of: thickness of a dielectric layer between the first and second reference planes; the relative dielectric constant of a dielectric layer between the first and second reference planes; the surface area of the first and second reference planes; the thickness of the conductive material of the first or second reference planes; the type of conductive material of the first or second reference planes; placement of discrete capacitors shunting the first and second reference planes; and the number of connections which a package including semiconductor circuits makes to a die and a printed circuit board having the dual referenced transmission line.

-3-

Serial No. 10/662,391
Appeal Brief Under 37 CFR 41.37 Filed February 14, 2006
Advisory Action dated November 1, 2005

9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

-4-

Serial No. 10/662,391
Appeal Brief Under 37 CFR 41.37 Filed February 14, 2006
Advisory Action dated November 1, 2005

10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.

-5-